Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-26 (Previously cancelled).

Claims 27-36 (Currently cancelled).

37. (Currently amended) An electrically programmable and erasable memory ~~[The]~~ device ~~[of claim 27, further]~~ comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions of a second conductivity type formed in the substrate, with a channel region therebetween;

an electrically conductive floating gate disposed vertically over and insulated from a portion of said channel region and a portion of the first region;

an electrically conductive source region electrically connected to the first region in the substrate, the source region having a lower portion that is disposed vertically over the first region and laterally adjacent to and insulated from the floating gate, and an upper portion that extends up and over the floating gate and terminates in a first end that is disposed vertically over and insulated from the floating gate;

an electrically conductive control gate having a first portion and a second portion, the first control gate portion being disposed laterally adjacent to and insulated from the floating gate, and the second control gate portion extends up and over the floating gate and terminates in a second end that is disposed vertically over and insulated from the floating gate;

wherein the first and second ends are disposed laterally adjacent to and insulated from each other such that no portion of the control gate is disposed directly between the floating gate and the source region; and

insulation material disposed directly between the first end and the floating gate, and having a thickness for permitting voltage coupling therebetween.

38. (Currently amended) An array of electrically programmable and erasable memory devices ~~[The device of claim 31, wherein each of the memory cell pairs further comprises]~~ comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions; and

each of the active regions including a column of pairs of memory cells extending in the first direction, each of the memory cell pairs including:

a first region and a pair of second regions spaced apart in the substrate and having a second conductivity type, with channel regions formed in the substrate between the first region and the second regions,

a pair of electrically conductive floating gates each disposed vertically over and insulated from a portion of one of the channel regions and a portion of the first region,

an electrically conductive source region electrically connected to the first region in the substrate, the source region having a lower portion that is disposed vertically over the first region and laterally adjacent to and insulated from the pair of floating gates, and an upper portion that extends up and over the floating gates and terminates in a pair of first ends that each is disposed vertically over and insulated from one of the floating gates,

a pair of electrically conductive control gates each having a first portion and a second portion, wherein for each of the control gates, the first control gate portion is disposed laterally adjacent to and insulated from one of the floating gates and the second control gate portion extends up and over the one floating gate and terminates in a second end that is disposed vertically over and insulated from the one floating gate,

wherein each of the first ends is disposed laterally adjacent to and insulated from one of the second ends such that no portion of the control gates is disposed directly between the floating gates and the source region, and

insulation material disposed directly between the first ends and the floating gates, and having a thickness for permitting voltage coupling therebetween.

Claim 39 (Currently cancelled).

40. (Currently amended) An electrically programmable and erasable memory ~~[The]~~ device ~~[of claim 39, further]~~ comprising:

a substrate of semiconductor material of a first conductivity type;

first and second spaced-apart regions of a second conductivity type formed in the substrate, with a channel region therebetween;

an electrically conductive floating gate disposed vertically over and insulated from a portion of said channel region and a portion of the first region;

an electrically conductive source region electrically connected to the first region in the substrate, the source region having a lower portion that is disposed vertically over the first region and laterally adjacent to and insulated from the floating gate, and an upper portion that extends up and over the floating gate and terminates in a first end that is disposed vertically over and insulated from the floating gate;

an electrically conductive control gate having a first portion and a second portion, the first control gate portion being disposed laterally adjacent to and insulated from the floating gate, and the second control gate portion extends up and over the floating gate and terminates in a second end that is disposed vertically over and insulated from the floating gate;

wherein the first and second ends are disposed laterally adjacent to and insulated from each other such that there is no vertical overlap between the control gate and the source region;

insulation material disposed directly between the source region lower portion and the floating gate, and having a thickness permitting voltage coupling therethrough; and

insulation material disposed directly between the first end and the floating gate, and having a thickness permitting voltage coupling therethrough.

41. (Previously amended) The device of claim 40, further comprising:

insulation material disposed directly between the floating gate and the second end, and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.

Claims 42 (Currently cancelled).

43. (Currently amended) The device of claim ~~[42]~~ 44, wherein each of the source regions extends across the active regions and isolation regions in a second direction substantially perpendicular to the first direction and intercepts one of the memory cell pairs in each of the active regions.

44. (Currently amended) An array of electrically programmable and erasable memory devices ~~[The device of claim 42, wherein each of the memory cell pairs further comprises]~~ comprising:

a substrate of semiconductor material of a first conductivity type;

spaced apart isolation regions formed on the substrate which are substantially parallel to one another and extend in a first direction, with an active region between each pair of adjacent isolation regions; and

each of the active regions including a column of pairs of memory cells extending in the first direction, each of the memory cell pairs including:

a first region and a pair of second regions spaced apart in the substrate and having a second conductivity type, with channel regions formed in the substrate between the first region and the second regions,

a pair of electrically conductive floating gates each disposed vertically over and insulated from a portion of one of the channel regions and a portion of the first region,

an electrically conductive source region electrically connected to the first region in the substrate, the source region having a lower portion that is disposed vertically over the first region and laterally adjacent to and insulated from the pair of floating gates, and an upper portion that extends up and over the floating gates and terminates in a pair of first ends that each is disposed vertically over and insulated from one of the floating gates,

a pair of electrically conductive control gates each having a first portion and a second portion, wherein for each of the control gates, the first control gate portion is disposed laterally adjacent to and insulated from one of the floating gates and the second control gate portion extends up and over the one floating gate and terminates in a second end that is disposed vertically over and insulated from the one floating gate, and wherein each of the first ends is disposed laterally adjacent to and insulated from one of the second ends such that there is no vertical overlap between the control gates and the source region,

insulation material disposed directly between the source region lower portion and the pair of floating gates, and having a thickness permitting voltage coupling therethrough, ~~[,]~~ and

insulation material disposed directly between the the first ends and the floating gates, and having a thickness permitting voltage coupling therethrough.

45. (Previously amended) The device of claim 44, wherein each of the memory cell pairs further comprises:

insulation material disposed directly between the floating gates and the second ends, and having a thickness permitting Fowler-Nordheim tunneling of charges therethrough.